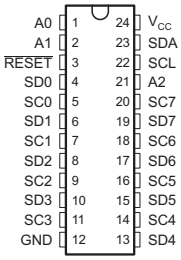
LOW VOLTAGE 8-CHANNEL I²C SWITCH WITH RESET

Check for Samples: TCA9548A

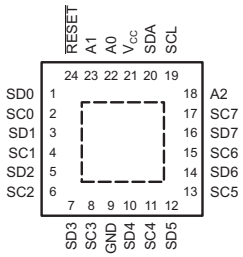
FEATURES

- 1-of-8 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Active-Low Reset Input
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Channel Selection Via I²C Bus
- Power-Up with All Switch Channels Deselected
- Low r_{ON} Switches
- Allows Voltage-Level Translation Between 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V-Tolerant Inputs
- 400-kHz Fast I²C Bus
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

PW PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TCA9548A has eight bidirectional translating switches that can be controlled via the I²C bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register.

The system master can reset the TCA9548A in the event of a timeout or other improper operation by asserting a low in the RESET input. Similarly, the power-on reset deselects all channels and initializes the I²C/SMBus state machine. Asserting RESET causes the same reset/initialization to occur without powering down the part.

The pass gates of the switches are constructed so that the V_{CC} pin can be used to limit the maximum high voltage, which is passed by the TCA9548A. This allows the use of different bus voltages on each pair, so that 1.8-V or 2.5-V or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5-V tolerant.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGE	Reel of 3000	TCA9548ARGER	
	TSSOP – PW	Reel of 2000	TCA9548APWR	PW548A
		Tube of 60	TCA9548APW	

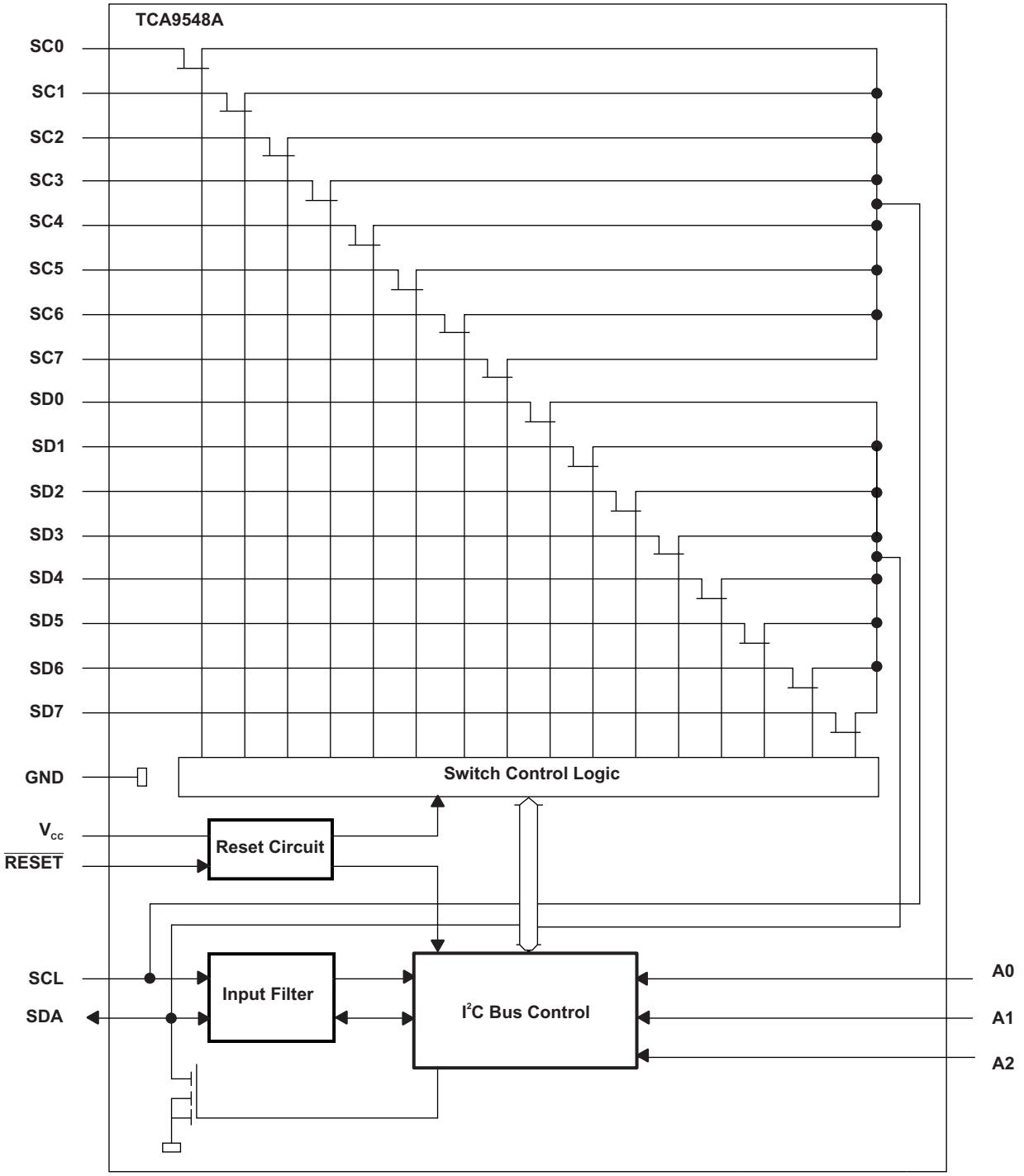
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NO.		NAME	DESCRIPTION
TSSOP (PW)	QFN (RTW)		
1	22	A0	Address input 0. Connect directly to V_{CC} or ground.
2	23	A1	Address input 1. Connect directly to V_{CC} or ground.
3	24	$\overline{RESET}$	Active-low reset input. Connect to V_{CC} through a pull-up resistor, if not used.
4	1	SD0	Serial data 0. Connect to V_{CC} through a pull-up resistor.
5	2	SC0	Serial clock 0. Connect to V_{CC} through a pull-up resistor.
6	3	SD1	Serial data 1. Connect to V_{CC} through a pull-up resistor.
7	4	SC1	Serial clock 1. Connect to V_{CC} through a pull-up resistor.
8	5	SC2	Serial data 2. Connect to V_{CC} through a pull-up resistor.
9	6	SC2	Serial clock 2. Connect to V_{CC} through a pull-up resistor.
10	7	SD3	Serial data 3. Connect to V_{CC} through a pull-up resistor.
11	8	SC3	Serial clock 3. Connect to V_{CC} through a pull-up resistor.
12	9	GND	Ground
13	10	SD4	Serial data 4. Connect to V_{CC} through a pull-up resistor.
14	11	SC4	Serial clock 4. Connect to V_{CC} through a pull-up resistor.
15	12	SD5	Serial data 5. Connect to V_{CC} through a pull-up resistor.
16	13	SC5	Serial clock 5. Connect to V_{CC} through a pull-up resistor.
17	14	SD6	Serial data 6. Connect to V_{CC} through a pull-up resistor.
18	15	SC6	Serial clock 6. Connect to V_{CC} through a pull-up resistor.
19	16	SD7	Serial data 7. Connect to V_{CC} through a pull-up resistor.
20	17	SC7	Serial clock 7. Connect to V_{CC} through a pull-up resistor.
21	18	A2	Address input 2. Connect directly to V_{CC} or ground.
22	19	SCL	Serial clock bus. Connect to V_{CC} through a pull-up resistor.
23	20	SDA	Serial data bus. Connect to V_{CC} through a pull-up resistor.
24	21	V_{CC}	Supply voltage

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

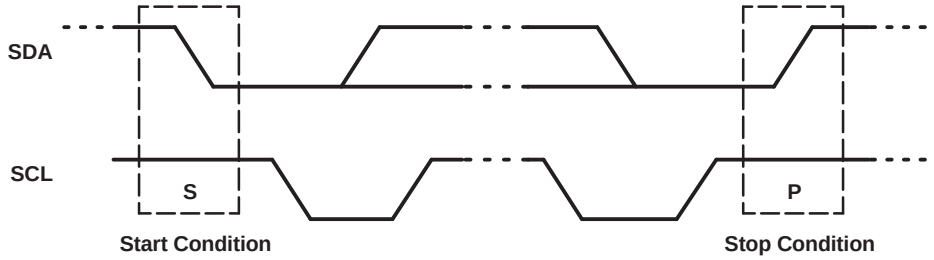


Figure 1. Definition of Start and Stop Conditions

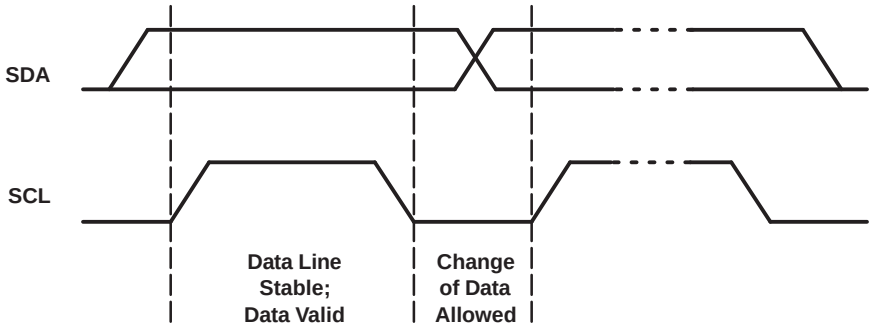


Figure 2. Bit Transfer

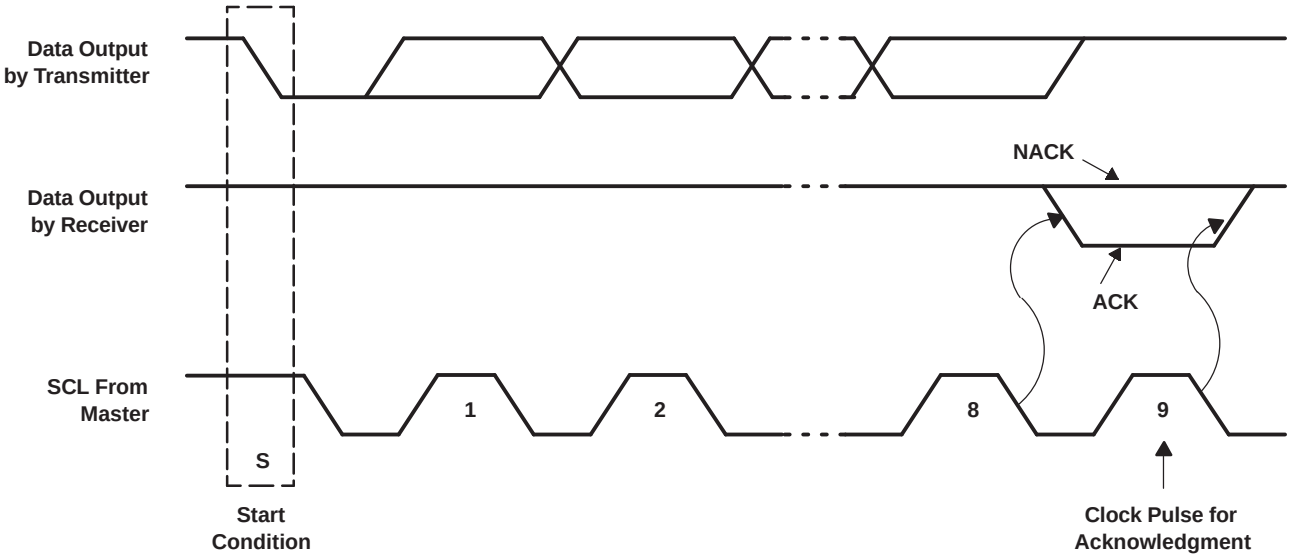


Figure 3. Acknowledgment on I^2C Bus

Device Address

Figure 4 shows the address byte of the TCA9548A.

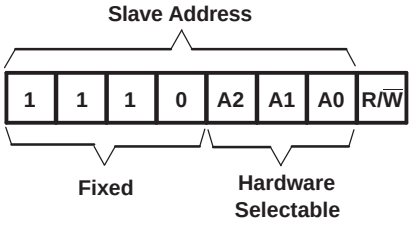


Figure 4. TCA9548A Address

Table 1. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Control Register

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9548A (see Figure 5). This register can be written and read via the I^2C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the TCA9548A, it saves the last byte received.

Channel Selection Bits (Read/Write)

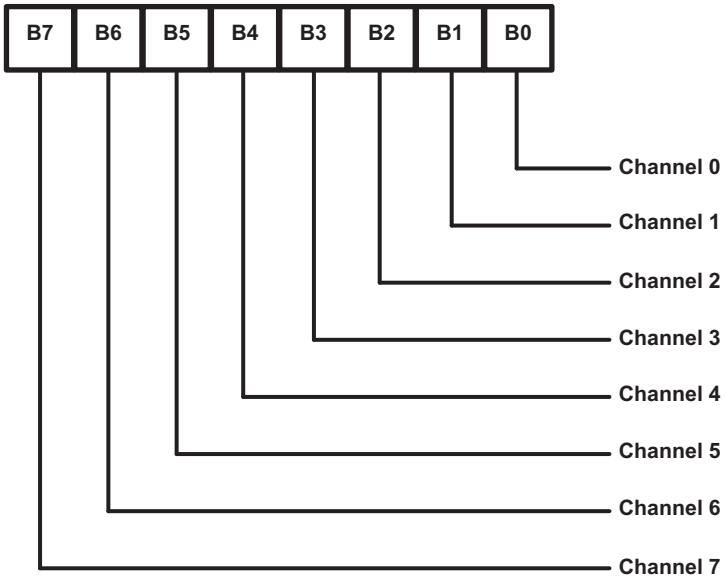


Figure 5. Control Register

Table 2. Command Byte Definition

CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL}, the TCA9548A resets its registers and I^2C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA9548A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the TCA9548A registers and I^2C state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Voltage Translation

The pass-gate transistors of the TCA9548A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another. Figure 6 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using the data specified in the *Electrical Characteristics* section of this data sheet).

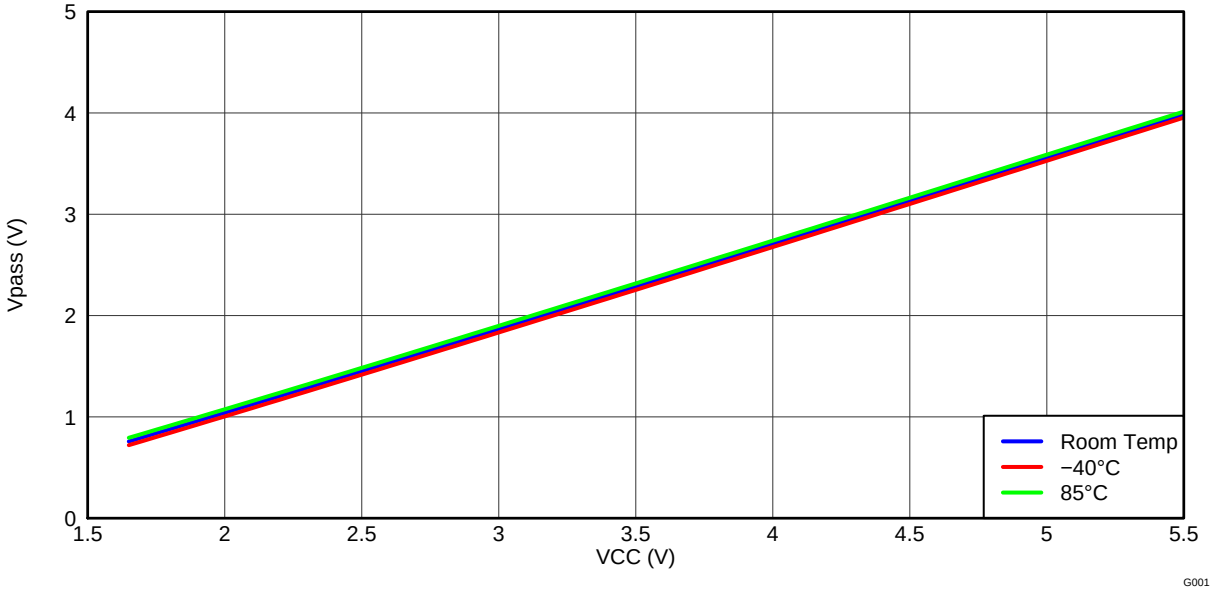


Figure 6. Pass-Gate Voltage vs Supply Voltage at Three Process Points

For the TCA9548A to act as a voltage translator, the $V_{o(sw)}$ voltage must be equal to, or lower than, the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 6, $V_{o(sw)}$(max) is 2.7 V when the TCA9548A supply voltage is 3.5 V or lower, so the TCA9548A supply voltage can be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 11).

Bus Transactions

Data is exchanged between the master and TCA9548A through write and read commands.

Writes

Data is transmitted to the TCA9548A by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which SCn/SDn channel receives the data that follows the command byte (see Figure 7). There is no limitation on the number of data bytes sent in one write transmission.

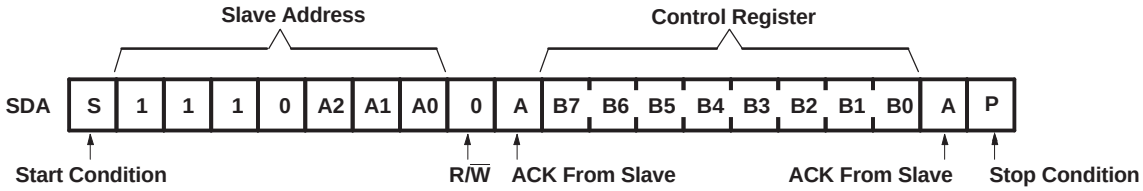


Figure 7. Write to Control Register

Reads

The bus master first must send the TCA9548A address with the LSB set to a logic 1 (see Figure 4 for device address). The command byte is sent after the address and determines which SCn/SDn channel is accessed. After a restart, the device address is sent again, but this time, the LSB is set to a logic 1. Data from the SCn/SDn channel defined by the command byte then is sent by the TCA9548A (see Figure 8). After a restart, the value of the SCn/SDn channel defined by the command byte matches the SCn/SDn channel being accessed when the restart occurred. Data is clocked into the SCn/SDn channel on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

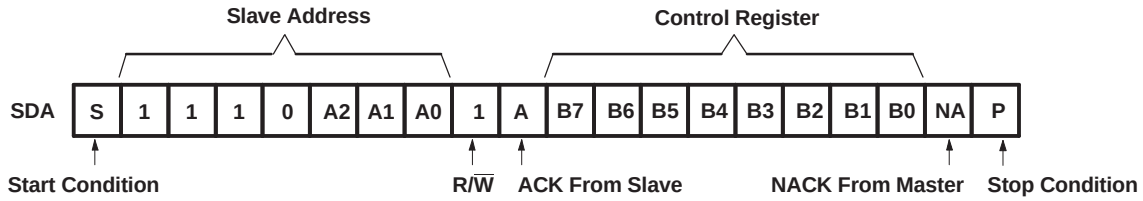


Figure 8. Read From Control Register

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
I_I	Input current			±20	mA
I_O	Output current			±25	mA
I_{CC}	Supply current			±100	mA
θ_{JA}	Package thermal impedance, junction to free air(3)	PW package		88	°C/W
		RTW package		45	
θ_{JP}	Package thermal impedance, junction to pad	RTW package		1.5	°C/W
T_{stg}	Storage temperature range		–65	150	°C
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	6	V
		A2–A0, $\overline{\text{RESET}}$	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A2–A0, $\overline{\text{RESET}}$	–0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature		–40	85	°C

Electrical Characteristics

V_{CC} = 2.3 V to 3.6 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{POR}	Power-on reset voltage(2)		No load, $V_I = V_{CC}$ or GND	1.65 V to 5.5 V		1.6	2.1	V
$V_{o(sw)}$	Switch output voltage		$V_{i(sw)} = V_{CC}$, I_{SWout} = –100 µA	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1		2	
				1.8 V		1.1		
				1.65 V to 1.95 V	0.9		1.25	
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 5.5 V	3	6		mA
			V_{OL} = 0.6 V		6	9		
I_I	SCL, SDA		$V_I = V_{CC}$ or GND	1.65 V to 5.5 V			±1	µA
	SC7–SC0, SD7–SD0						±1	
	A2–A0						±1	
	$\overline{\text{RESET}}$						±1	
I_{CC}	Operating mode	f_{SCL} = 400 kHz	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V		50	80	µA
				3.6 V		20	35	
				2.7 V		11	20	
				1.65 V		6	10	
		f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V		9	30	
				3.6 V		6	15	
				2.7 V		4	8	
				1.65 V		2	4	
	Standby mode	Low inputs	V_I = GND, I_O = 0	5.5 V		0.2	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
				1.95 V		0.1	1	
		High inputs	$V_I = V_{CC}$, I_O = 0	5.5 V		0.2	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
				1.95 V		0.1	1	
ΔI_{CC}	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND	1.65 V to 5.5 V		3	20	µA
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			3	20	
C_i	A2–A0		$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		4	5	pF
	$\overline{\text{RESET}}$					4	5	
	SCL		$V_I = V_{CC}$ or GND, Switch OFF			20	28	
$C_{io(off)}$ (3)	SDA		$V_I = V_{CC}$ or GND, Switch OFF	1.65 V to 5.5 V		20	28	pF
	SC7–SC0, SD7–SD0					5.5	7.5	
r_{on}	Switch-on resistance		V_O = 0.4 V, I_O = 15 mA	4.5 V to 5.5 V	4	10	20	Ω
				3 V to 3.6 V	5	12	30	
			V_O = 0.4 V, I_O = 10 mA	2.3 V to 2.7 V	7	15	45	
				1.65 V to 1.95 V	10	25	70	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.
(2) The power-on reset circuit resets the I^2C bus logic with $V_{CC} < V_{POR}$. V_{CC} must be lowered to 0.2 V to reset the device.
(3) $C_{io(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0 (1)		0 (1)		µs
t_{icr}	I²C input rise time			1000	20 + 0.1C_b (2)	300	ns
t_{icf}	I²C input fall time			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C output (SDn) fall time (10-pF to 400-pF bus)			300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low) (3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high) (3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 10)

Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 9)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{rst} (2)	$\overline{\text{RESET}}$ time (SDA clear)		$\overline{\text{RESET}}$	SDA		500	ns

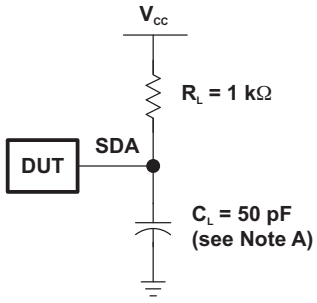
(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

Reset Timing Requirements

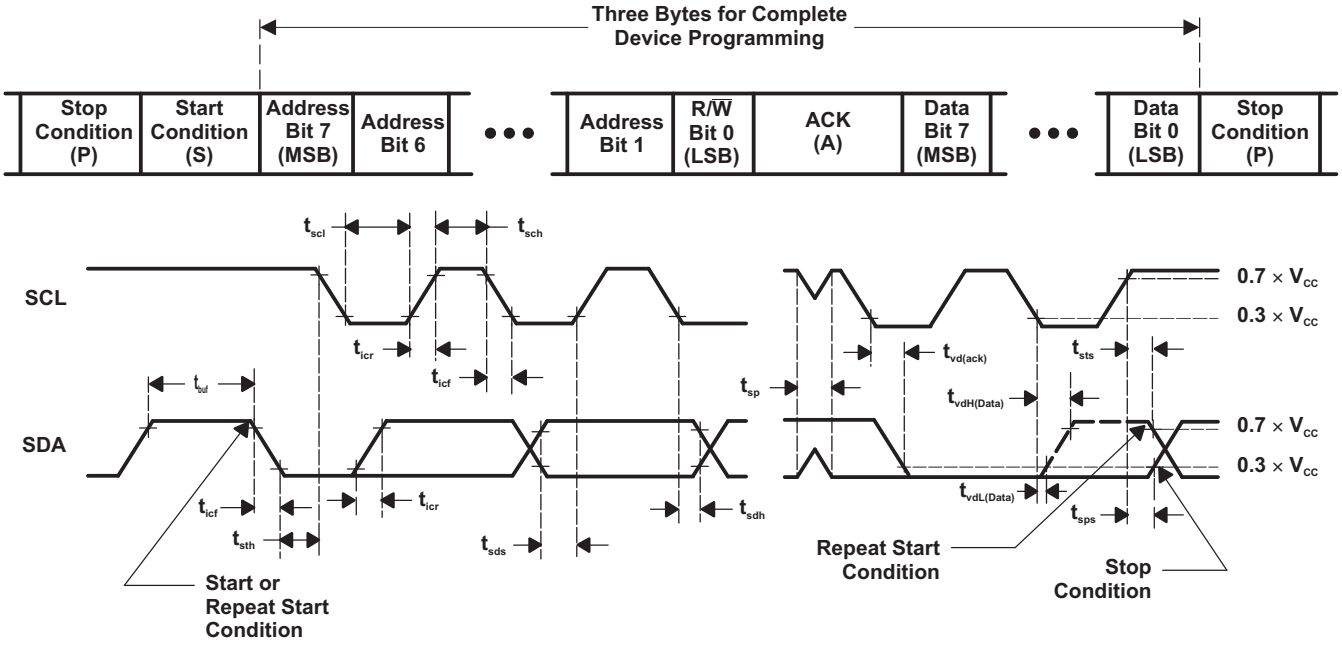
over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{W(L)}$	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

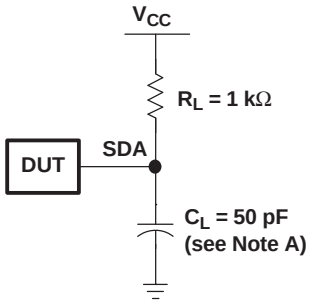
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

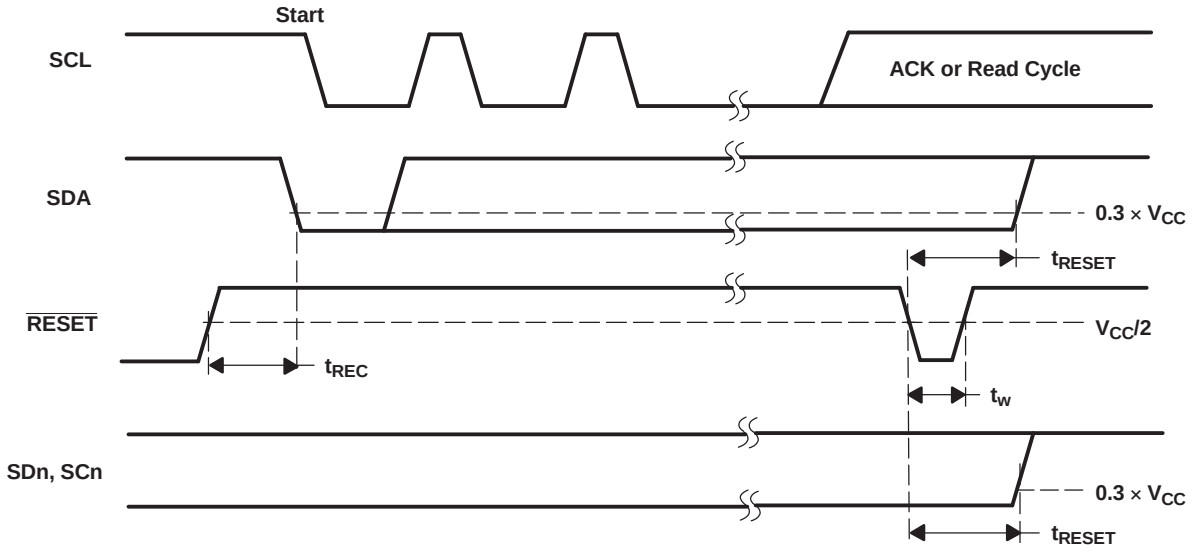
C. Not all parameters and waveforms are applicable to all devices.

Figure 9. I^2C Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

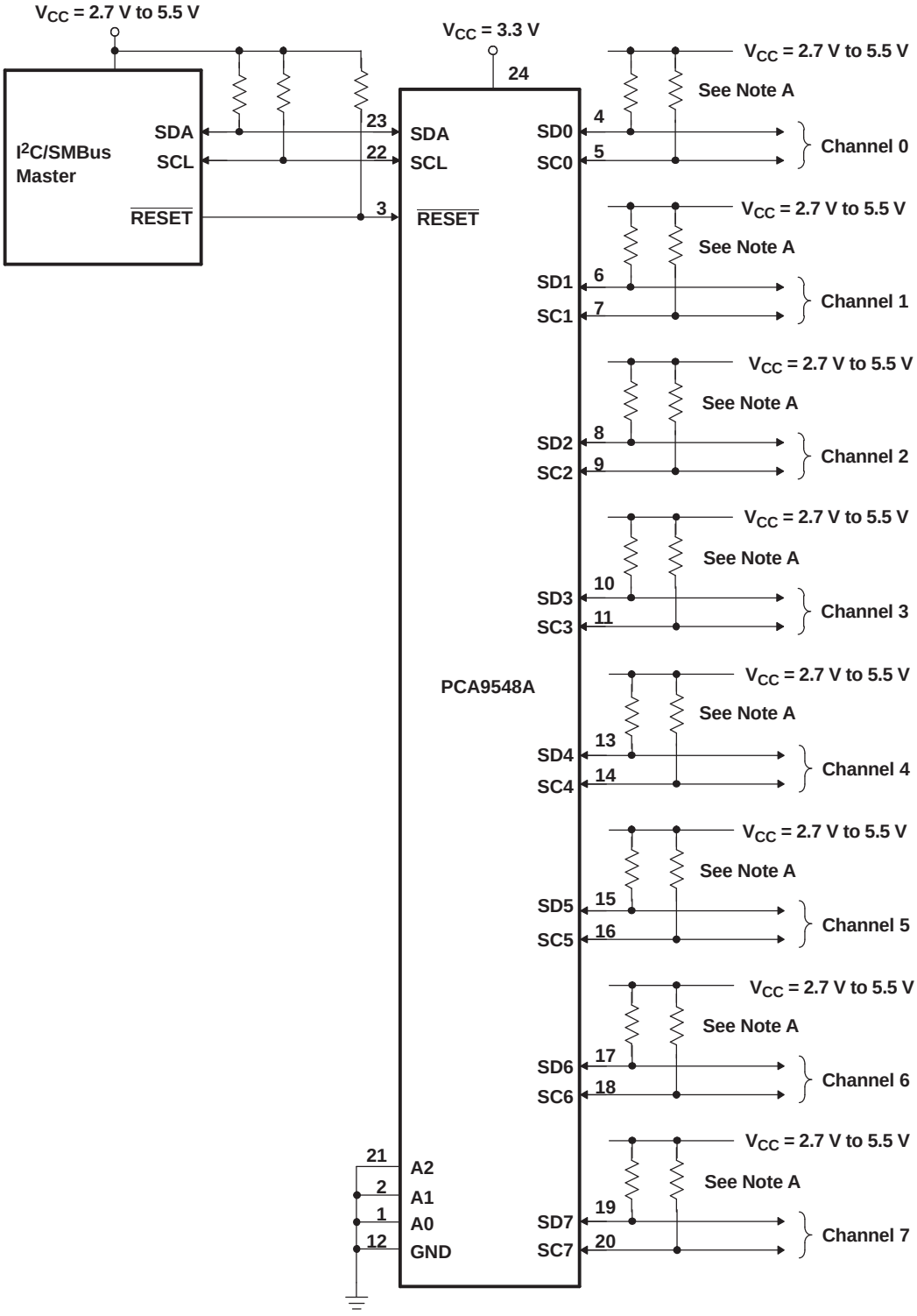
C. I/Os are configured as inputs.

D. Not all parameters and waveforms are applicable to all devices.

Figure 10. Reset Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 11 shows an application in which the TCA9548A can be used.



A. Pin numbers shown are for the PW and RTW packages.

Figure 11. Typical Application

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9548A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 12 and Figure 13.

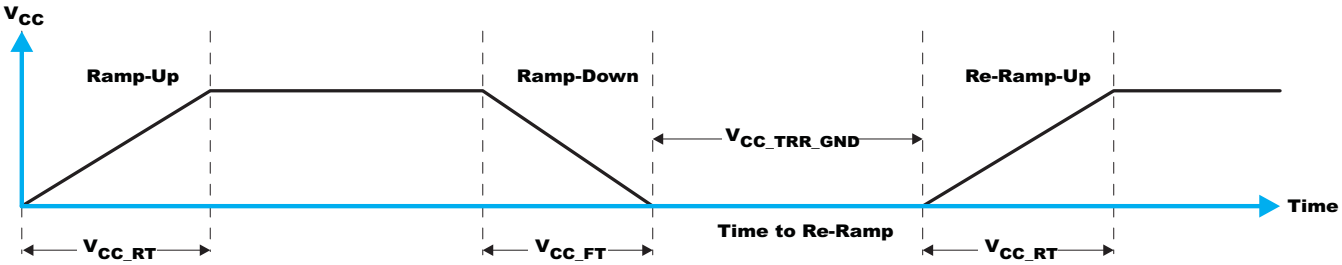


Figure 12. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

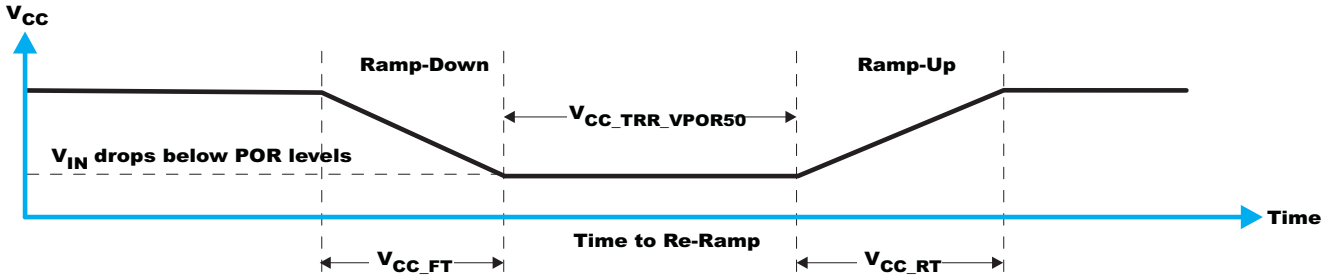


Figure 13. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 3 specifies the performance of the power-on reset feature for TCA9548A for both types of power-on reset.

Table 3. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 12	1		100	ms
V_{CC_RT}	Rise rate	See Figure 12	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 12	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See Figure 13	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 14			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 14				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on fising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 14 and Table 3 provide more information on how to measure these specifications.

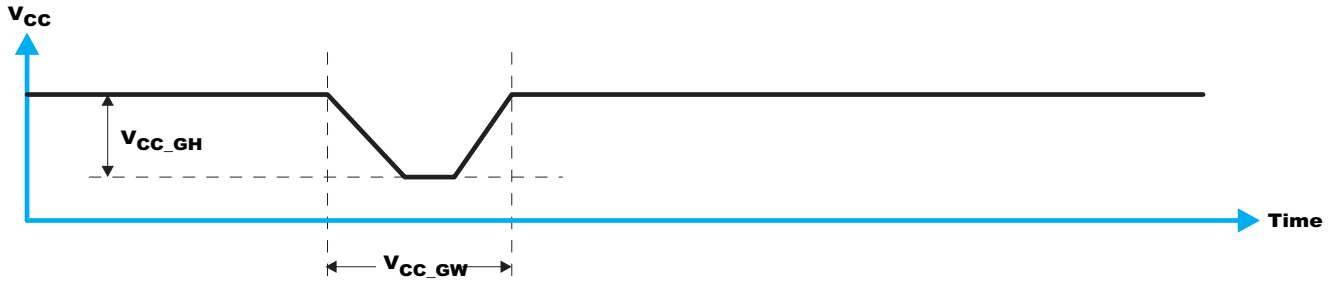


Figure 14. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 15 and Table 3 provide more details on this specification.

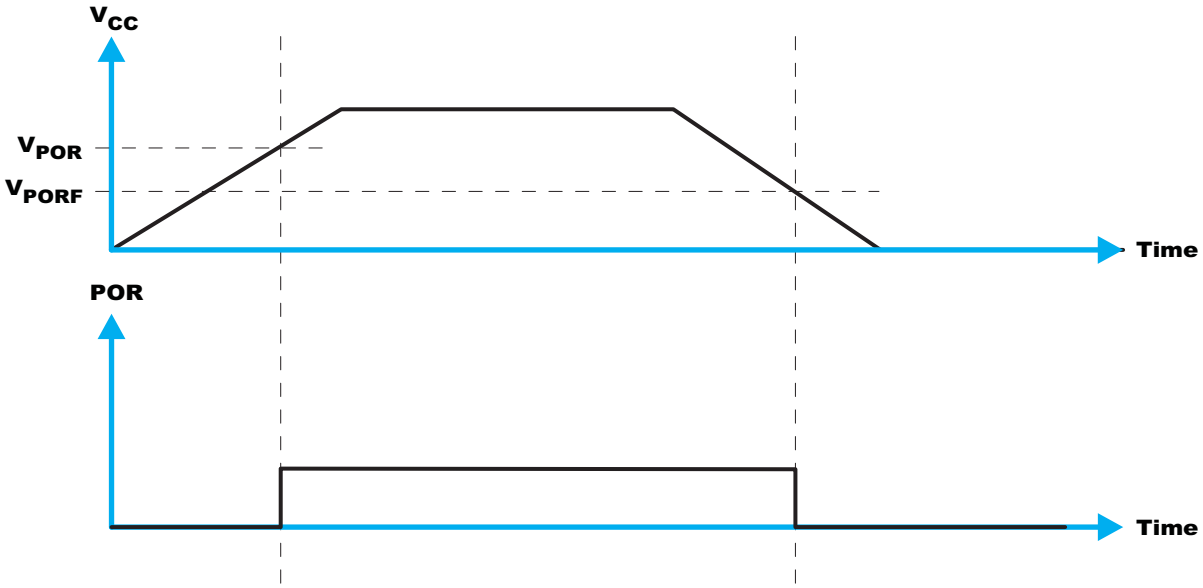


Figure 15. V_{POR}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9548APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A	Samples
TCA9548ARGER	PREVIEW	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

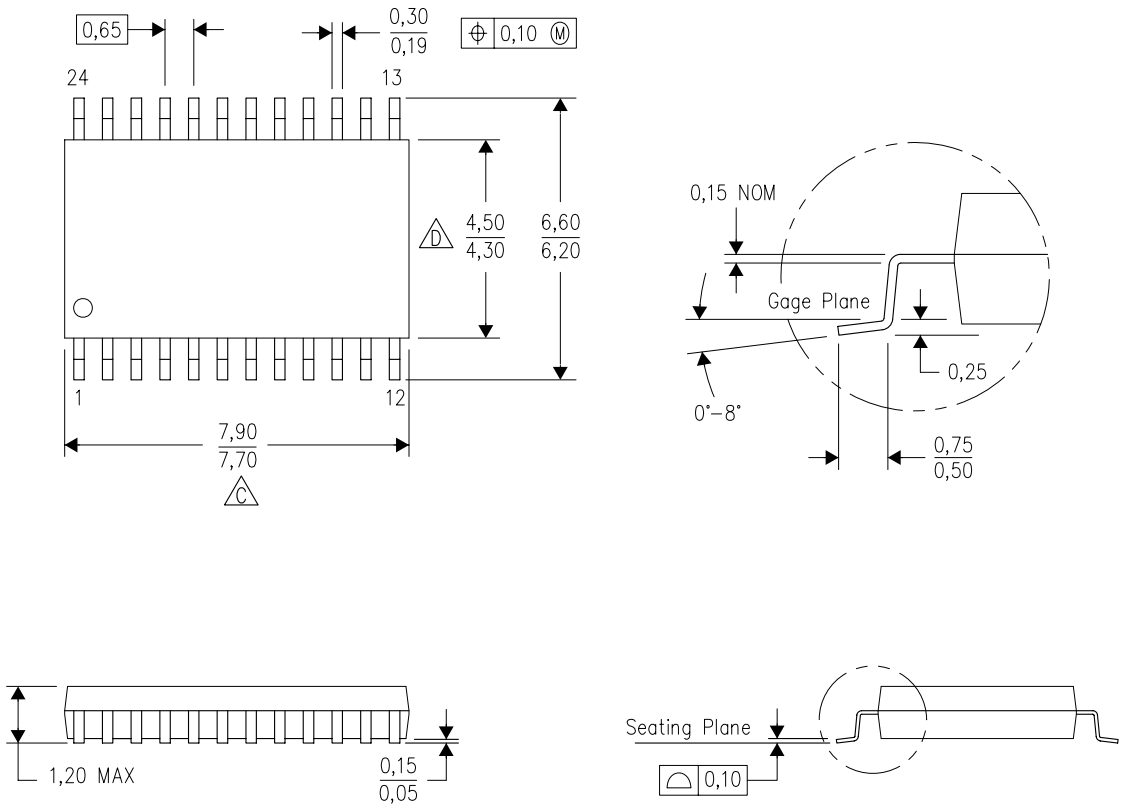
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

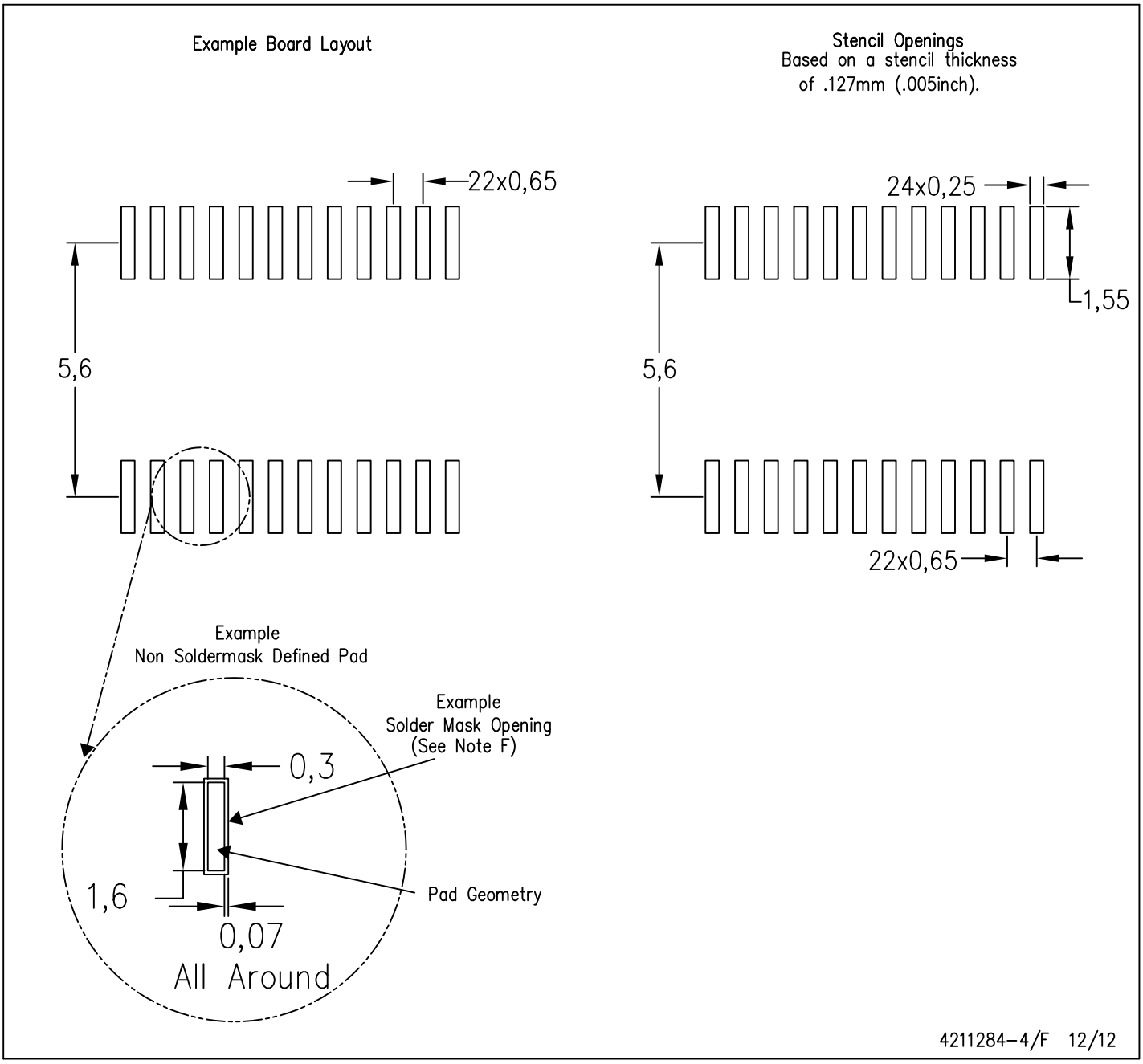
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

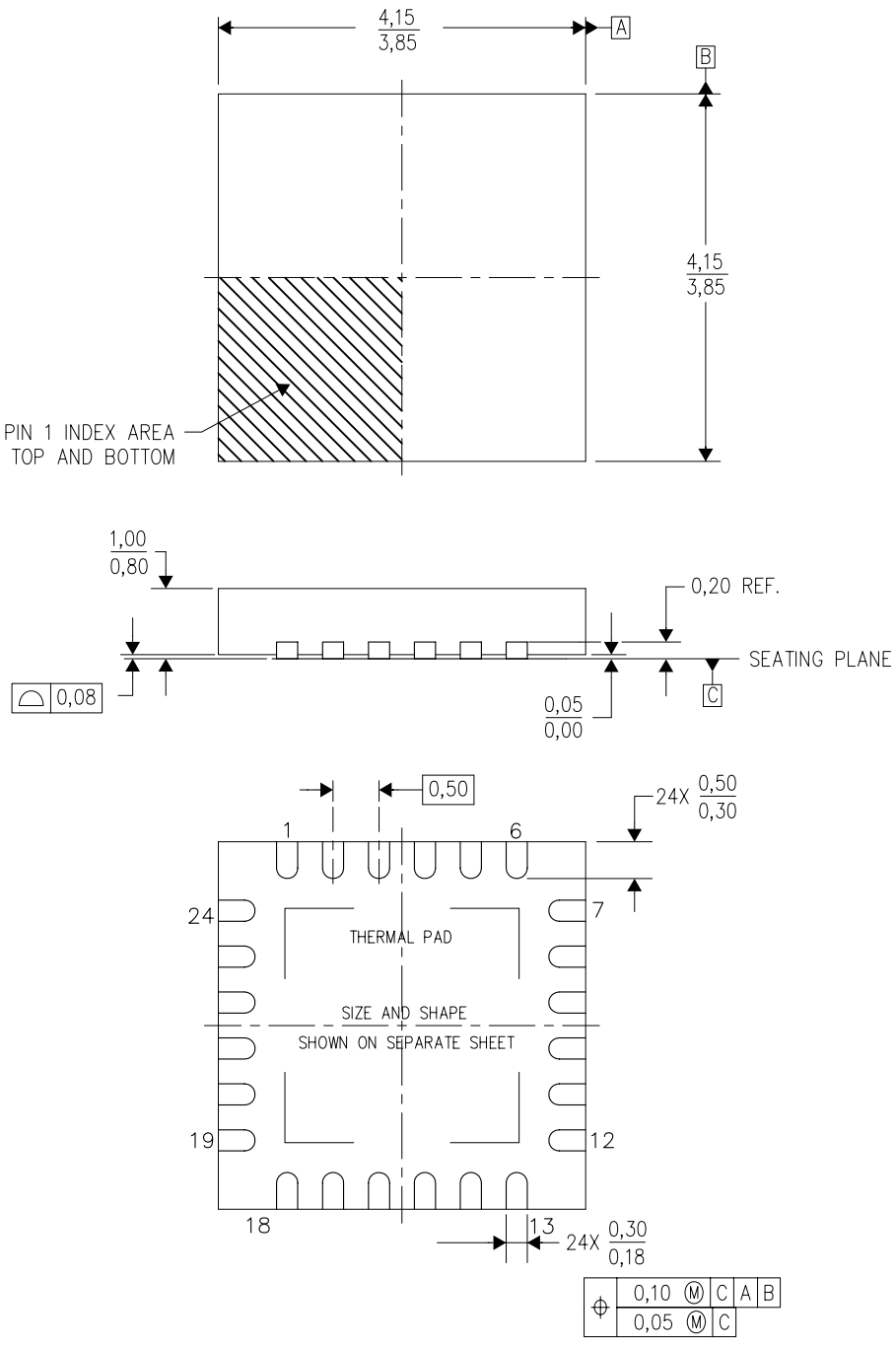
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

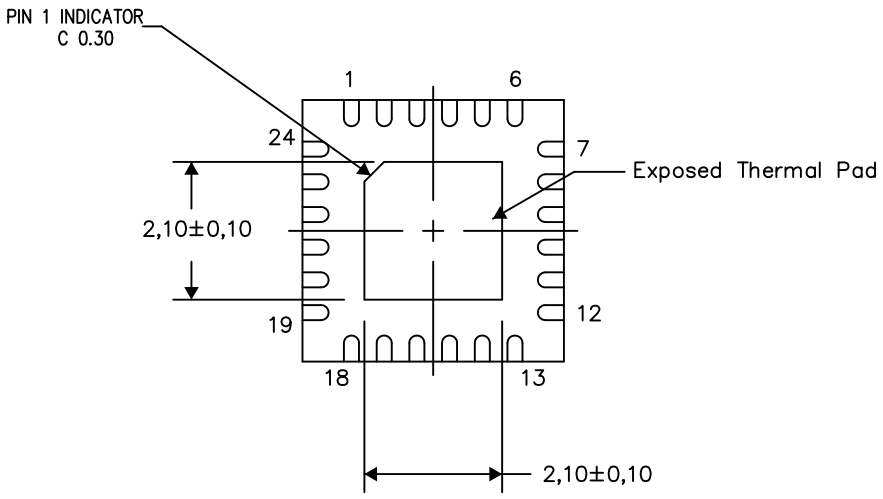
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



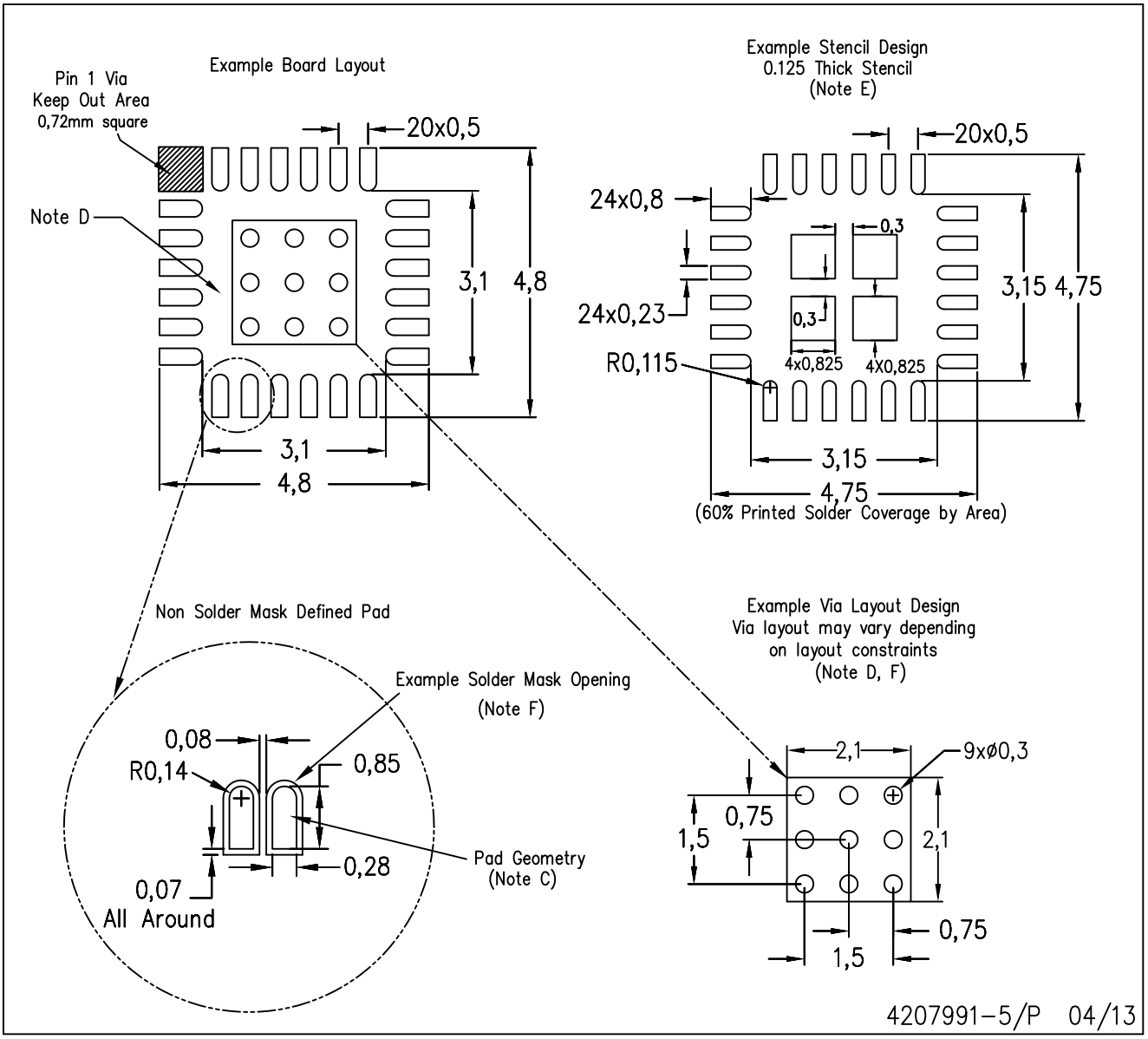
Bottom View

Exposed Thermal Pad Dimensions

4206344–6/AD 04/13

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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